

IN THE CLAIMS**Listing of Claims:**

- 1 1. (currently amended) A receiver comprising:
2 an oscillator outputting three or more phases of a clock signal; and
3 a retiming mechanism coupled to said oscillator having circuitry for receiving
4 said phases of said clock signal, ~~circuitry for receiving~~ and serial data, and circuitry
5 operable to reduce timing uncertainties in said serial data by outputting a value of said
6 serial data sampled at a particular phase of said clock signal.

- 1 2. (currently amended) The receiver as recited in claim 1, wherein said retiming
2 mechanism comprises a plurality of first units, wherein each of said plurality of first
3 units comprises circuitry for sampling said serial data using a said particular phase of
4 said clock signal.

- 1 3. (currently amended) The receiver as recited in claim 2, wherein each of said
2 plurality of first units comprises circuitry for receiving said particular phase of said
3 clock signal and a complement of said particular phase of said clock signal and said
4 serial data.

- 1 4. (currently amended) The receiver as recited in claim 2, wherein said retiming
2 mechanism further comprises a plurality of second units, wherein each of said
3 plurality of second units is associated with a particular first unit, wherein each of said
4 plurality of second units comprises circuitry for outputting the value of said
5 serial data sampled by said associated first unit upon activation.

1 5. (original) The receiver as recited in claim 4, wherein a particular second unit of
2 said plurality of second units is activated based on a logical state of each input to said
3 particular second unit.

1 6. (currently amended) The receiver as recited in claim 5, wherein said logical state
2 of each input is determined based on combinational logic using said phases of said
3 clock signal and complements of said phases of said clock signal.

1 7. (currently amended) A system comprising:
2 a transmission medium;
3 a transmitter coupled to said transmission medium configured to convert
4 parallel data to a serial form; and
5 a receiver coupled to said transmission medium, wherein said receiver
6 comprises:
7 an oscillator outputting three or more phases of a clock signal; and
8 a retiming mechanism coupled to said oscillator having circuitry for
9 receiving said phases of said clock signal, ~~circuitry for receiving~~ and serial data, and
10 circuitry operable to reduce timing uncertainties in said serial data by outputting a
11 value of said serial data sampled at a particular phase of said clock signal.

1 8. (currently amended) The system as recited in claim 7, wherein said retiming
2 mechanism comprises a plurality of first units, wherein each of said plurality of first
3 units comprises circuitry for sampling said serial data using a said particular phase of
4 said clock signal.

1 9. (currently amended) The system as recited in claim 8, wherein each of said
2 plurality of first units comprises circuitry for receiving said particular phase of said
3 clock signal and a complement of said particular phase of said clock signal and said
4 serial data.

1 10. (currently amended) The system as recited in claim 8, wherein said retiming
2 mechanism further comprises a plurality of second units, wherein each of said
3 plurality of second units is associated with a particular first unit, wherein each of said
4 plurality of second units comprises circuitry for outputting [[a]] the value of said
5 serial data sampled by said associated first unit upon activation.

1 11. (original) The system as recited in claim 10, wherein a particular second unit of
2 said plurality of second units is activated based on a logical state of each input to said
3 particular second unit.

1 12. (currently amended) The system as recited in claim 11, wherein said logical state
2 of each input is determined based on combinational logic using said phases of said
3 clock signal and complements of said phases of said clock signal.